ABSTRACT:

A clock strategy is provided for digital circuits inside mixed-signal ICs. An integrated circuit in accordance with the present invention comprises a plurality of pairs of latches (L1, L2) being respectively clocked by two non-overlapping clock signals (Φ1, Φ2). The clock strategy is aimed at keeping the substrate bounce caused by the digital circuits as low as possible. Preferably, not all latches are clocked at the same time, but delays are inserted in the clock lines so that the various latches do not consume current all at the same time. The invention relaxes the demands on the substrate sensitivity of the analog circuits.

(Fig. 3)